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RN-6801

B. E. - III (Sem. V) (Ele.) Examination

May / June - 2010

Digital Circuits

(Old Course)

Time : 3 Hours]

[Total Marks : 100

Instructions :

(1)

नीचे दृशविले निशानीवाणी विगतो उत्तरवही पर अवश्य लखवी. Fillup strictly the details of signs on your answer book.	Seat No. :
Name of the Examination :	<input type="text"/>
<input type="text" value="B. E. - 3 (Sem. 5) (Ele.)"/>	<input type="text"/>
Name of the Subject :	<input type="text"/>
<input type="text" value="Digital Circuits (Old)"/>	<input type="text"/>
Subject Code No. : <input type="text" value="6"/> <input type="text" value="8"/> <input type="text" value="0"/> <input type="text" value="1"/>	<input type="text" value="Student's Signature"/>
Section No. (1, 2,.....) : <input type="text" value="1&2"/>	

(2) Figures to the right indicate full marks.

(3) Make suitable assumptions wherever necessary.

SECTION - I

1 (a) Answer the following questions : 10

- (i) Binary equivalent of gray code 101 is _____.
- (ii) Demultiplexer has _____ input and _____ output.
- (iii) In the Karnaugh map of a function (A, B, C, D) consists of four variables, then total number of cell are _____.
- (iv) The 2's complement of 1011 is _____.
- (v) ASCII code is a _____ bit code.
- (vi) $\bar{A} + \bar{B} + \bar{C} = D$ represents a _____ gate.
- (vii) IC 7486 consists of four two input _____ gates.
- (viii) Each individual term in the standard SOP form is called as _____.

(ix) A half adder is also known as _____ gate.

(x) It is _____ to use IC 7483 as a subtractor

(a) Possible (b) Not possible

(b) Answer the following :

(i) Design full subtractor using half subtractor. **5**

(ii) Prove that $(A + \bar{B} + AB)(A + \bar{B})(\bar{A}B) = 0$

2 Answer the following :

(a) Perform the following : **4**

(i) $(54)_{10} - (22)_{10}$ in BCD using 10's complement.

(ii) $(0011.1001)_2 - (0001.1110)_2$ using is complement. **4**

(b) Realize a digital circuit for following function. **7**

$$Y = \sum m (1, 5, 7, 9, 11, 13, 15)$$

OR

2 (a) Convert decimal 46 to Gray code. **5**

(b) Realize following function using NAND gates only. **5**

$$Y = (\bar{A}B + \overline{A+B}) A\bar{B}$$

(c) Design a BCD adder using two 4 bit address. **5**

3 (a) Answer any **two** from following : **12**

(i) Draw and design 2 bit magnitude comparator circuit.

(ii) Design AND OR Ex-OR gate using NAND gate.

(iii) Divide $(101101)_2$ by $(110)_2$.

(b) How are binary and octal numbers related? **3**

SECTION - II

- 4 (a) Answer the following : 4
- (i) What is the output of the flip flop when $\overline{\text{CLR}} = 0$.
 - (ii) What do you mean by toggling?
 - (iii) What do you mean by lock out condition?
 - (iv) What is race-around condition?
- (b) Explain D type positive edge-triggered FF using NAND gate when $\text{CP} = 0$. 6
- (c) State true or false : 4
- (i) The set input can never be used to make Q a 0.
 - (ii) In asynchronous counter the clock pulse is common to each flip flop.
 - (iii) The Q output of D flip flop is not same as the input.
 - (iv) A single flip flop may be used to divide the input frequency by 4.
- (d) Explain the gated SR latch flip flop. 6
- 5 (a) Design a JK synchronous counter that goes through states 3,4,6,7 and 3..... Is the counter self-starting? 8
- (b) Design 4 bit binary ripple counter. 7
- OR**
- 5 (a) Design a multiplexer for the function 8
- $$F(A, B, C) = \sum(1, 3, 5, 6).$$
- Select A as input lines.
Use 4 * 1 mux.
- (b) Explain 2 bit register with parallel load. 7
- 6 Answer any two : 15
- (a) Explain clocked master slave flip flop
 - (b) Convert SR FF to D FF
 - (c) Design a mod-10 asynchronous counter using T FFs.